23.2 Circuit Design Issues in Multi-Gate FET CMOS Technologies

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Multi-Gate Field Effect Transistors (MuGFET) such as FinFETs [1] and Triple-Gate FETs [2] are promising device structures for sub-45nm CMOS technology nodes. The superior control of the channel due to multiple gates reduces short-channel effects and leakage currents. Circuit performance benefits from novel gate-stack materials, reduced parasitic capacitances, and hole mobility improvement. While previous work has primarily focused on device performance [1-3], this paper addresses the link between circuit design and technology. Digital and analog circuits are fabricated in an experimental MuGFET CMOS technology using standard Unibond SOI wafers. This work explores the impact of the three-dimensional device topology on CMOS circuit functionality, performance, and power dissipation. Here, relaxed FinFET and Triple-Gate device dimensions down to 55nm gate lengths and 30nm fin widths were chosen to increase yield and homogeneity for an early circuit investigation during device development. Fabrication of tall Triple-Gate FETs with 10nm fin width demonstrates the long-term scalability (Fig. 23.2.1). The major difference between Triple-Gate FET and FinFET is a third gate on top of the silicon fin. This allows for higher device currents [4] and relaxed process requirements, because the improved channel control of Triple-Gate FETs enables the use of larger fin widths at the same off-current specification.

In CMOS logic, the three-dimensional device topology in combination with a small fin pitch in multi-fin devices (Fig. 23.2.2) improves the circuit density compared to bulk CMOS technologies. This enables a larger effective transistor width (W_{EFF}) on the same footprint. Fabrication of these multi-fin devices, controlled by a common gate, is mandatory to adjust the driving strength and the nFET/pFET current ratio in logic gates. The discrete transistor widths of multi-fin MuGFETs are a circuit design limitation compared to bulk CMOS. Our investigations show that this design limitation is not critical for nFET/pFET sizing in CMOS logic circuits, especially for a <110> channel surface orientation. For this orientation the nFET and pFET drive currents are nearly equal, due to a higher hole mobility and slightly reduced electron mobility, which improves overall circuit performance. However, discrete transistor widths are a concern for SRAM cells, which are, in contrast to logic, composed of single-fin devices. While in bulk CMOS the optimization of cell noise margins for sub-1V SRAM is achieved by fine-tuning of the W/L ratios, the drive currents of single-fin MuGFETs can be modified only by different gate lengths.

Performance, active and leakage currents of FinFET and Triple-Gate FET based CMOS logic circuits are measured using 24 ring oscillator (RO) modules. The ROs are composed of various CMOS logic gates up to NAND3/NOR3 complexity with a fan out of two (FO2) and different device dimensions. Each RO module contains about 500 devices and includes a 10-stage frequency divider using edge-triggered master slave flip-flops. Triple-Gate circuits using TiN metal gate electrodes are 65% faster than FinFET circuits with Poly-Si gate electrodes at V_{DD}=1.2V (Fig. 23.2.3). The delays of the TiN-based Triple-Gate circuits are comparable to a production low power 90nm bulk-CMOS technology (V_T=350mV), which has a thinner gate oxide. Replacing the TiN gate material by TiSiN is essential to provide symmetric nFET and pFET V_T's. This is a key step for circuit design in a 32nm low power target process since it reduces the pFET V_T by 300mV compared to TiN gate material and further improves performance. An excellent sub-1V operation and a FO2-inverter delay of 21ps at V_{DD}=1.2V is demonstrated for scaled devices with 55nm gate lengths and 30nm fin widths. This corresponds to a 15ps FO1-inverter delay.

Low power circuits require additional high-V_T devices to implement non-critical paths in CMOS logic, large SRAMs, and sleep transistors to switch-off non-active circuit blocks. To study possible multi-V_T approaches, the trade-off between average off-current of an inverter stage and gate delay in FinFET ROs using devices with different gate lengths and fin widths is characterized (Fig. 23.2.4). Lowest off-currents are achieved for 80nm fin width and 110nm gate length because V_T increases in wider fins due to the channel doping. For a 32nm low standby power CMOS technology, devices with sub-100pA/μm off-currents require a further downscaling of the fin width to 20nm. The target V_T of 350mV is defined by the metal gate work-function, because channel doping is no longer possible. Combining the TiSiN single mid-gap gate material with the investigated dual gate length approach is attractive to provide circuits with different performance classes. Without increasing process complexity, fast circuits are based on devices with minimum gate lengths while leakage sensitive circuits are made of devices with longer gate lengths but smaller off-currents. Two different metal gate work-functions are definitely required for high-speed CMOS circuits to implement low-V_T nFETs and pFETs with V_T = 150mV.

Considering SoC integration capabilities, Fig. 23.2.5 shows a FinFET-based Miller OpAmp and the measured frequency response representing analog building blocks [5]. The low-frequency open loop gain is A_0 = 45dB. The 2pF capacitor is a planar MOS-structure and the bias resistor is made of poly-Si. Due to the large multi-fin transistors with non-minimum gate lengths, the effect of discrete device widths on circuit design is negligible. Metal gates with undoped fins are especially valuable in analog circuit design and SRAMs to reduce doping-induced V_T mismatch.

Figure 23.2.6 shows an I/O circuit concept based on co-integration of planar, partially depleted MOSFET (PD-SOI) devices and MuGFETs. This offers a solution to the electrostatic discharge (ESD) sensitivity of MuGFETs. MuGFETs show a low ESD current capability and high ESD sensitivity since device failure occurs instantaneously after breakdown at V_{FD} [6]. This motivates the co-integration of more robust PD-SOI devices for ESD clamps and multi-fin MuGFETs to provide large currents for fast I/O drivers.

Figure 23.2.7 gives a general overview of various SoC integration aspects. Our methodology to explore basic circuits in an early phase along with technology development reduces the risk, resulting from the three-dimensional device structure in combination with novel gate-stack materials.

References:

[1] S. Tang et al., "FinFET-A Quasi Planar Double Gate Transistor," *ISSCC Dig. Tech Papers*, pp. 118-119, Feb., 2001.
[2] B. Doyle et al., "Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout," *Dig. Symp. VLSI Technology*, pp. 133-134, 2003.
[3] N. Collaert et al., "A Functional 41-Stage Ring Oscillator Using Scaled FinFET Devices," *IEEE El. Dev. Let.*, vol. 25, no. 8, pp. 568-570, Aug., 2004.
[4] J.-P. Colinge, "Novel Gate Concepts for MOS Devices," *ESSDERC,* pp. 45-49, 2004.
[5] G. Knoblinger et al., "Design and Evaluation of Basic Analog Circuits in an Emerging MuGFET Technology," *IEEE SOI Conf.,* pp. 39-40, Oct., 2005.
[6] C. Russ et al., "ESD Evaluation of the Emerging MuGFET Technology," *EOS/ESD Symp.*, pp, 280-289, Sept., 2005.

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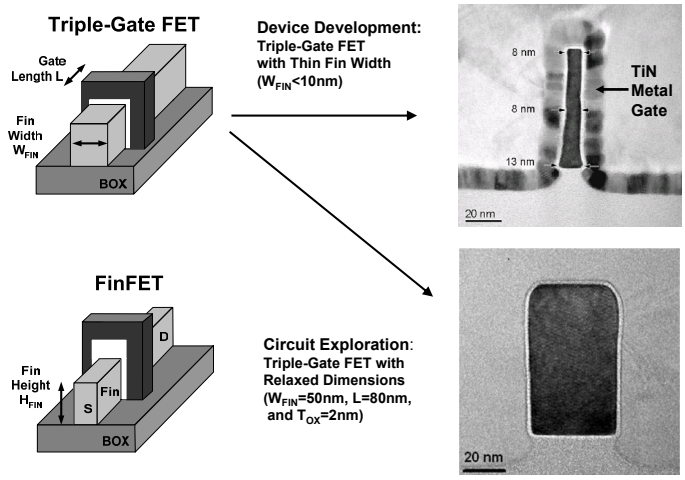
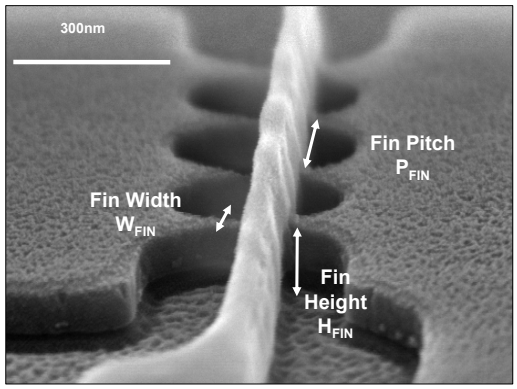


Figure 23.2.1: Multi-Gate FET structures and device parameters for circuit design.



FinFET: $W_{EFF} = 2\ n\ H_{FIN}$

Triple-Gate FET: $W_{EFF} = n\ (2\ H_{FIN} + W_{FIN})$

Footprint: $W_{FP} = n\ P_{FIN}$

Area gain over bulk CMOS: $W_{EFF}/\ n\ P_{FIN} > 1$

Figure 23.2.2: Basic multi-fin MuGFET device properties and their impact on circuit density.

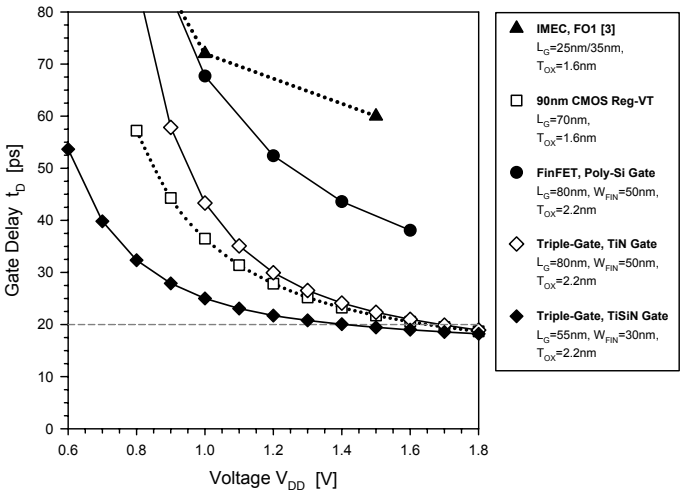


Figure 23.2.3: Measured delays of FinFET and Triple-Gate FET ring oscillators with fan out of two.

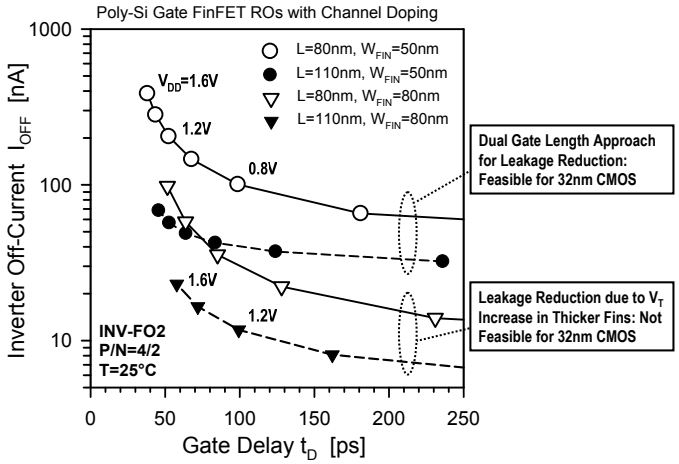


Figure 23.2.4: Leakage-performance trade-offs for different multi-V_T approaches in FinFET circuits.

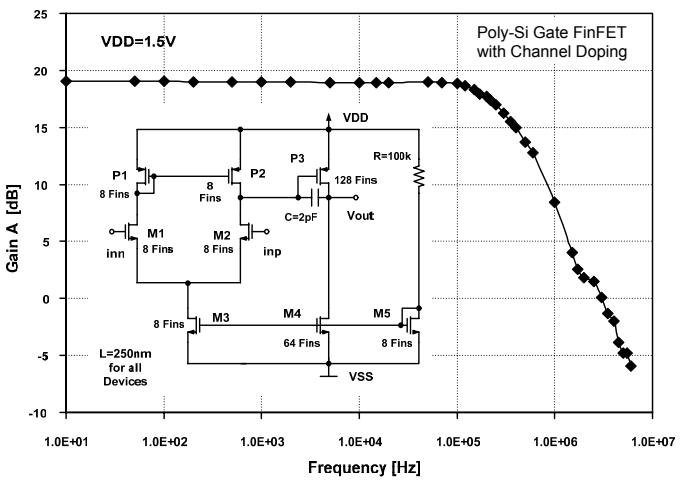


Figure 23.2.5: OpAmp and measured frequency response, configured as a 20dB inverting amplifier.

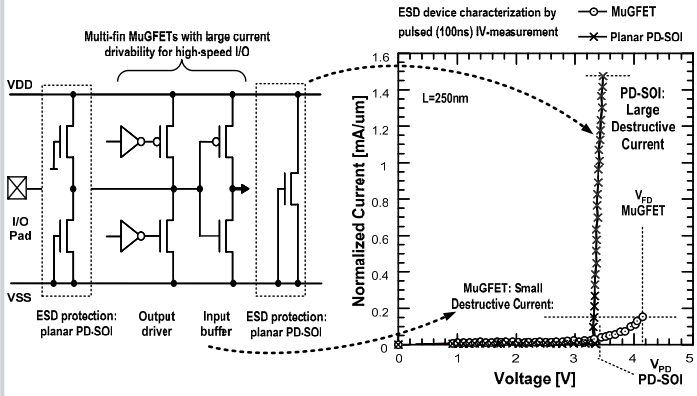


Figure 23.2.6: I/O circuit concept based on planar co-integration of MuGFETs and PDSOI.

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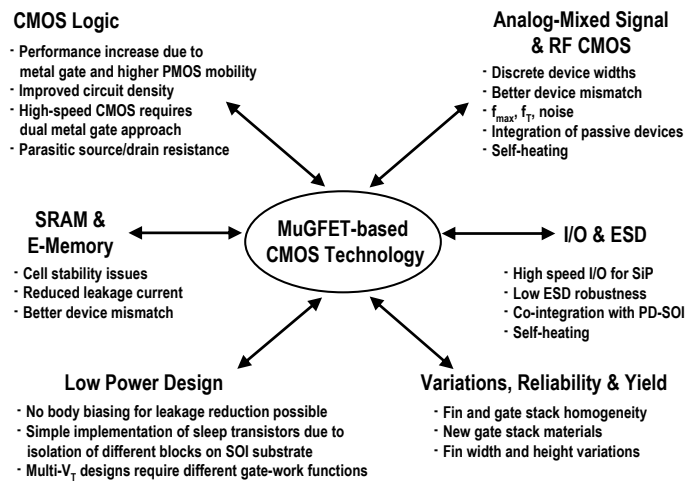

Figure 23.2.7: Impact of MuGFET-based CMOS technology on SOC integration aspects.

